FERROELECTRIC MEMORY DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a ferroelectric memory device, and more particularly relates to measures taken to improve the reliability thereof.

Over the past few years, portable communications terminals, IC cards and the like have been rapidly popularized around the world. To operate these types of electronic units more efficiently, nonvolatile semiconductor memory devices for use in these units are increasingly required to operate at an even lower voltage and at an even higher speed while consuming even lower power. A ferroelectric memory device is one of strong candidate nonvolatile memory devices that are expected to fulfill these requirements at the same time. A device of this type includes a ferroelectric capacitor, in which a ferroelectric film is sandwiched between a pair of electrodes. Data can be stored thereon in a nonvolatile manner depending on whether the ferroelectric material within the capacitor is polarized in one direction or the other, which is reversed by the application of a positive or negative electric field. In rewriting data stored on a ferroelectric memory device, such an electric field as reversing the direction of polarization in the ferroelectric film has only to be applied. Accordingly, the ferroelectric memory

device can advantageously contribute to higher-speed operation with lower voltage applied and lower power dissipated.

Figure **4** is a plan view of an array of memory cells in a conventional ferroelectric memory device as viewed from above its layer in which bit lines are formed. Figure **5** is a vertical cross-sectional view of part of the array taken along the line **V-V** in Figure **4**.

As shown in Figure **5**, an active region **OD** is formed to be surrounded by a LOCOS film **52** on an Si substrate **51**. Within this active region **OD**, source/drain doped layers **53**, and polysilicon gates **54** are formed. A first interlevel dielectric film **55** is formed over the Si substrate **51**. Memory cell capacitors are formed at respective regions over the LOCOS film **52** on the first interlevel dielectric film **55**. Each of these memory cell capacitors includes: a bottom electrode **56** made of a metal such as platinum or iridium; a ferroelectric film **57** made of a ferroelectric material; and a top electrode **58** also made of a metal such as platinum or iridium. A second interlevel dielectric film **59** is formed over the first interlevel dielectric film **55**. And storage lines **60**, made of aluminum containing copper, are formed on the second interlevel dielectric film **59**.

In Figure **4**, the gates **54** and bottom electrodes **56** extend along the rows of the array as word lines **WL0, WL1, WL2** and **WL3** and cell plate lines **CP0, CP1, CP2** and **CP3**, respec-

tively. A group of bit lines **BL0, /BL0, BL1, /BL1, DBL** and **/DBL** are formed to extend along the columns of the array. One of these bit lines, i.e., a bit line **DBL**, is illustrated in Figure **5** by a phantom line. Each top electrode **58** shown in Figure **5** corresponds to a data storage node of a DRAM, and is identified by **TE** in Figure **4**. Each storage line **60** is connected to an associated top electrode **58** via a contact **CE** and to an associated doped layer **53** of the memory cell transistor via a contact **CW1**. Each bit line **BL0, /BL0, BL1, /BL1, DBL** or **/DBL** is connected to an associated doped layer **53** via a contact **CW2**. And the respective storage lines **60** and the group of bit lines **BL0, /BL0, BL1, /BL1, DBL** and **/DBL** constitute a first interconnection layer.

In this device, data can be retained as either "0" or "1" by holding a ferroelectric film **57** in either positively or negatively polarized state depending on a level difference between a voltage on a bit line supplied via an associated doped layer **53** and a voltage on an associated cell plate line.

The reliability of this ferroelectric memory device sometimes deteriorates due to the infant mortality failure of the ferroelectric capacitor or degradation in retention characteristics thereof. The present inventors carried out intensive research to find out measures to be taken for solving this problem. As a result of experiments, we obtained data

suggesting that the decrease in reliability might have been brought about probably because a storage line **60** exists over an excessively wide range above an associated top electrode **58** of a ferroelectric capacitor.

SUMMARY OF THE INVENTION

An object of the present invention is providing a ferroelectric memory device with improved reliability, in which the deterioration in characteristics of a ferroelectric capacitor can be eliminated by controlling an overlap area between a storage line and an underlying top electrode in a planar layout.

To achieve this object, the present invention adopts a structure in which a first interconnection layer does not cover at least one side of each top electrode of a memory cell in the planar layout thereof.

A ferroelectric memory device according to the present invention includes a ferroelectric capacitor including a top electrode having a rectangular planar pattern, a bottom electrode, and a ferroelectric film interposed between the top and bottom electrodes. The memory device further includes a memory cell transistor including first and second doped layers and a gate. The memory cell transistor is used for controlling a voltage supplied to the top electrode of the ferroelectric capacitor. The memory device further includes: an

interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor; and a first interconnection layer formed on the interlevel dielectric film. In the planar layout of the memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode.

In this structure, a stress applied by the first interconnection layer to the ferroelectric capacitor or a leakage current flowing between adjacent portions of the first interconnection layer decreases, thus preventing decrease in early yield resulting from leakage failure and deterioration in retention characteristics. As a result, the reliability of the ferroelectric memory device can be improved.

In one embodiment of the present invention, the first interconnection layer includes a storage line and a bit line. The storage line is connected to the top electrode of the ferroelectric capacitor and to the first doped layer of the memory cell transistor, and is linear in the planar pattern thereof. The bit line is connected to the second doped layer of the memory cell transistor. In this particular embodiment, the storage line may intersect only one side of the top electrode of the ferroelectric capacitor in the planar layout. Alternatively or additionally, the bit line may not overlap with the top electrode of the ferroelectric capacitor

in the planar layout.

In another embodiment of the present invention, the storage line may include: a first region connected to the top electrode of the ferroelectric capacitor; a second region connected to the first doped layer of the memory cell transistor; and a third region interposed between the first and second regions. The third region may intersect the side of the top electrode in the planar layout. The line width of the third region is preferably smaller than that of the first and second regions.

In such an embodiment, remarkable effects can be attained in respect of the stress reduction and so on.

In still another embodiment, the first interconnection layer is preferably made of a material containing at least one of aluminum and copper.

In still another embodiment, the ferroelectric memory device may further include: an upper interlevel dielectric film formed to cover the first interconnection layer; and a second interconnection layer formed on the upper interlevel dielectric film. The second interconnection layer may totally cover the top electrode of the ferroelectric capacitor in the planar layout.

In still another embodiment, the ferroelectric memory device may further include: an upper interlevel dielectric film formed to cover the first interconnection layer; and a

second interconnection layer formed on the upper interlevel dielectric film. The second interconnection layer may totally cover the bottom electrode of the ferroelectric capacitor in the planar layout.

In these embodiments, it is possible to prevent the characteristics of the ferroelectric capacitor from being deteriorated due to annealing conducted before the second interconnection layer is formed. In addition, the stress applied to the ferroelectric capacitor during the formation of the second interconnection layer can be relaxed.

In still another embodiment, the second interconnection layer is also preferably made of a material containing at least one of aluminum and copper.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure **1** is a plan view of a ferroelectric memory device according to a first embodiment of the present invention as viewed from above a first interconnection layer thereof.

Figure **2** is a cross-sectional view of the device taken along the line **II-II** in Figure **1**.

Figure **3** is a plan view of a ferroelectric memory device according to a second embodiment of the present invention as viewed from above a first interconnection layer thereof.

Figure **4** is a plan view of a conventional ferroelectric memory device as viewed from above a first interconnection

layer thereof.

Figure **5** is a cross-sectional view of the device taken along the line **V-V** in Figure **4**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

EMBODIMENT 1

Figure **1** is a plan view of an array of memory cells in a ferroelectric memory device according to a first embodiment of the present invention as viewed from above a layer in which bit lines are formed. Figure **2** is a vertical cross-sectional view of the device taken along the line **II-II** in Figure **1**.

As shown in Figure **2**, an active region **OD** is formed to be surrounded by a LOCOS film **12** on an Si substrate **11**. Within this active region **OD**, source/drain doped layers **13** and polysilicon gates **14** are provided. A first interlevel dielectric film **15** is formed over the Si substrate **11**. Memory cell capacitors are formed at respective regions over the LOCOS film **12** on the first interlevel dielectric film **15**. Each of these memory cell capacitors includes: a bottom electrode **16** made of a metal such as platinum or iridium; a ferroelectric film **17** made of a ferroelectric material described later; and a top electrode **18** also made of a metal such as platinum or iridium. A second interlevel dielectric film **19** is formed over the first interlevel dielectric film **15**. And

storage lines **20** made of aluminum containing copper are formed on the second interlevel dielectric film **19**.

In Figure **1**, the gates **14** and bottom electrodes **16** extend as word line **WL0**, **WL1**, **WL2** and **WL3** and cell plate lines **CP0**, **CP1**, **CP2** and **CP3**, respectively, along the rows of the array. A group of bit lines **BL0**, **/BL0**, **BL1**, **/BL1**, **DBL** and **/DBL** are formed to extend along the columns of the array. One of these bit lines, i.e., a bit line **DBL**, is illustrated in Figure **2** by a phantom line. Each top electrode **18** shown in Figure **2** corresponds to a data storage node of a DRAM, and is identified by **TE** in Figure **1**. Each storage line **20** is connected to an associated top electrode **18** via a contact **CE** and to an associated doped layer **13** of the memory cell transistor via a contact **CW1**. Each bit line **BL0**, **/BL0**, **BL1**, **/BL1**, **DBL** or **/DBL** is connected to an associated doped layer **13** via a contact **CW2**. And the respective storage lines **20** and the group of bit lines **BL0**, **/BL0**, **BL1**, **/BL1**, **DBL** and **/DBL** constitute a first interconnection layer.

In this device, data can be retained as either "0" or "1" by holding a ferroelectric film **17** in either positively or negatively polarized state depending on a level difference between a voltage on a bit line supplied via an associated doped layer **13** and a voltage on an associated cell plate line.

The ferroelectric memory device of the present invention

is characterized in that a storage line **20** overlaps with an associated top electrode (TE) **18** in a different planar area than that of the conventional structure. In the conventional ferroelectric memory device structure, the right end of each storage line **60** goes over an associated side of an underlying top electrode **58** to protrude outward as shown in Figure **5**. In the plan view shown in Figure **4**, each storage line **60** intersects two sides of an associated top electrode **58**. In contrast, in the ferroelectric memory device of the present invention, the right end of each storage line **20** does not protrude outward from an associated side of an underlying top electrode **18** as shown in Figure **2**. In the plan view shown in Figure **1**, each storage line **20** intersects only one side of an associated top electrode **18**. Furthermore, in the conventional structure shown in Figure **4**, each bit line covers another two sides of an associated pair of top electrodes **58**. On the other hand, according to the present invention, each bit line (e.g., **BL1**) is disposed not to overlap with any top electrode **20** in the planar layout of the device. In other words, as viewed from above, the first interconnection layer covers all of the four sides of each top electrode **60** in the conventional ferroelectric memory device shown in Figure **4**. In contrast, the first interconnection layer does not cover at least one side of each top electrode **18** in the inventive ferroelectric memory device shown in Figure **1**.

In a contact **CE** between a top electrode **18** and an associated storage line **20**, an overlap margin is defined at a minimum size according to a design rule in view of a mask-to-mask placement error between the contact **CE** and the storage line **20**.

By reducing in this way the overlap area between a storage line **20** and an associated top electrode **18** as much as possible, the following effects are attained. Specifically, it is possible to prevent the early yield from decreasing due to a leakage failure between a bit line and a storage line. In addition, the characteristics of the ferroelectric capacitor can be significantly improved in respect of data retention, in particular. This is because the polarizability of the ferroelectric capacitor can be improved. At present, these effects are attained probably because of the following reasons: decrease in stress applied by a storage line **20** to an associated ferroelectric capacitor; and/or reduction in leakage caused between a storage line **20** shorter in length and a neighboring bit line (e.g., **BL1**). Also, possibly, advantageous effects of a material for a third interlevel dielectric film (not shown), which is formed over the storage lines **20**, on the ferroelectric capacitors might be promoted with such a configuration.

It should be noted, however, so long as each storage line **20** covers only one side of an associated top electrode **18** (TE)

in the planar layout, an associated bit line may overlap with the top electrode **18**. Alternatively, in the planar layout, if each bit line (e.g., **BL1**) does not overlap with an associated top electrode **18**, then an associated storage line **20** may cover two sides of the top electrode **18**. Nevertheless, according to the illustrated embodiment, the stress applied by the first interconnection layer to the top electrode **18** can be reduced more significantly than any other possible alternative exemplified above, resulting in marvelous improvement of the retention characteristics.

Also, in this embodiment, dummy bit lines **DBL** and **/DBL** are disposed at the far ends of the array of memory cells so as not to use the ferroelectric capacitors at those ends during the operation of the device. This is because even with the structure of this embodiment, the characteristics might not be improved otherwise. Specifically, although a memory cell located at an end of the array has the same structure as any other memory cell within the array, the former cell is adjacent to a region where no cells exist, and therefore exhibits a different characteristic than that of the latter cell.

If the ferroelectric memory device is fabricated to further include: a third interlevel dielectric film formed over the storage lines **20**; and a second interconnection layer formed thereon (not shown), then that second interconnection

layer may cover the top or bottom electrodes **18** or **16**. In such a case, it is possible to prevent the characteristics of a ferroelectric capacitor from being deteriorated due to annealing conducted before the second interconnection layer is formed. In addition, the stress applied to the ferroelectric capacitor during the formation of the second interconnection layer can be relaxed.

Particularly when the second interconnection layer is made of a material containing aluminum and/or copper, the following effects are attained. The second interconnection layer may be used as a backing layer for reducing the resistance of a word line (e.g., **WL0**, **WL1**) made of polysilicon and/or a cell plate line (e.g., **CP0**, **CP1**), which is the bottom electrode **16** of the ferroelectric capacitor. Since the resistance can be reduced, the ferroelectric memory device can operate at a higher speed. In addition, even if a word line is disconnected during a manufacturing process, electrical failures are less likely to happen, because the second interconnection layer, serving as a backing layer, are connected at numerous points.

EMBODIMENT 2

Figure **3** is a plan view of an array of memory cells according to a second embodiment of the present invention as viewed from above its layer in which bit lines are formed.

The ferroelectric memory device of the second embodiment is characterized in that the overlap area between each storage line **20** and an associated top electrode **18** (TE) is even smaller than that in the first embodiment. Specifically, as shown in Figure **3**, each storage line **20** has such a planar shape that the line width of the central region thereof is smaller than that of the other regions thereof. The line width of the central region is defined at the minimum value according to a design rule for forming the storage line. In the other respects, the structure of the second embodiment is the same as that of the first embodiment.

In the ferroelectric memory device of the second embodiment, the overlap area between each storage line **20** and an associated top electrode **18** is further reduced as compared to the ferroelectric memory device of the first embodiment. Accordingly, the effects of the first embodiment can be attained more remarkably.

In the second embodiment, a second interconnection layer may also be formed over the storage lines **20** with a third interlevel dielectric film interposed therebetween as described in the first embodiment.

It should be noted, however, so long as each storage line **20** covers only one side of an associated top electrode **18** (TE) in the planar layout, an associated bit line may overlap with the top electrode **18**. Alternatively, in the planar layout, if

each bit line (e.g., **BL1**) does not overlap with an associated top electrode **18**, then an associated storage line **20** may cover two sides of the top electrode **18**. Nevertheless, according to the illustrated embodiment, the stress applied by the first interconnection layer to the top electrode **18** can be reduced more significantly than any other possible alternative exemplified above, resulting in marvelous improvement of the retention characteristics.

In the foregoing embodiments, the ferroelectric film **17** may be made of a ferroelectric material selected from the group consisting of KNO_3, $PbLa_2O_3-ZrO_2-TiO_2$ and $PbTiO_3-PbZrO_3$.